Multicellular processor based on MCp042R100102 die in LQFP-256 plastic package

Brand mark*	Processor core - 4 cells	Architecture	Temperature range	Order
MCp042R100102 LQ 256 I	MCc042R1	Multicellular	-40°C... + 125°C	Submit order
MCp042R100102 LQ 256 M	MCc042R1	Multicellular	- 60°C... + 125°C	Submit order

*brand mark of multicellular cores and processors

MULTICLET R1 is a principally new product of R series (Reconfiguration). It has the ability of dynamic reconfiguration.

Only processors with multicellular architecture perform dynamic reconfiguration during task algorithm execution. As a result of such feature, core cells can simultaneously solve different tasks. This is implemented in MULTICLET R1 processor core by setting flow control scheme before task execution.

In the process of task execution programmer can involve from 1,2,3 or 4 cells, while uninvoled cells can perform other tasks.

Dynamic Reconfiguration reduces power consumption. Below are the estimates for power consumption at work a different number of cells when regulating of the frequency of PLL.

On the task of FFT

60MHz:
0 cells - 183 mA (0.183 mA * 1.8V = 0.33 W)
1 cell - 230 mA (0.41 W)
4 cells - 348 mA (0.63 W)

30MHz:
0 cells - 102 mA (0.18 W)
1 cell - 128 mA (0.23 W)
4 cells - 191 mA (0.34 W)

On a mix 75% DMAC + 25%ADD (Typical Sine Wave Data Switching)

60MHz:
0 cells - 150 mA (0,15 mA * 1,8V = 0,2
1 cell - 195 mA (0,35 W)
4 cells - 210 mA (0,38 W)

30MHz:
0 cells - 75 mA (0,13 W)
1 cell - 97 mA (0,17 W)
4 cells - 105 mA (0,19 W)

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8 MHz:
0 cells - 38 mA (0.07 W)
1 cell - 45 mA (0.08 W)
4 cells - 63 mA (0.11 W)

8 MHz:
0 cells - 20 mA (0,04 W)
1 cell - 26 mA (0,05 W)
4 cells - 28 mA (0,05 W)

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