MULTICLET P1

Processor core MULTICLET P1 is oriented at maximum **P**erformance and simultaneous reduction of pow
basis of multicellular architecture, which gives the core properties of natural implementation of parallelism
process. MULTICLET P1 is fully synthesizable.

Nomenclature	Implementation	Description
MCc040P1	FPGA	4-cells, 16/32bit, fixed point processor core contains ALU in each cel Calculated value of power consumption on 180nm is 213 umW/MHz
MCc041P1	SoC	4-cells, 32/64bit FPU processor core contains ALU in each cell. Perf Power consumption on 180nm is 9 mW/MHz.
MCc042P1	RTL	4-cells, 32/64bit, double precision FPU multicellular processor core c the core is 24 MFlops/MHz. Calculated value of power consumption
MCc080P1	RTL	8-cells, 32bit, fixed point multicellular processor core contains ALU in 8 MIPS/MHz. Calculated value of power consumption on 180nm is 4
MCc162P1	RTL	16-cells, 64bit, double precision FPU multicellular processor core co MCc162P1 is 96 MFlops/MHz. Calculated value of power consumpti

MULTICLET P2

Processor core MULTICLET P2 is oriented at maximum **P**erformance and simultaneous reduction of pow
basis of multicellular architecture, which gives the core properties of natural implementation of parallelism
process. MULTICLET P2 is fully synthesizable.

Nomenclature	Implementation	Description
MCc042P2	RTL	4-cells, 32/64bit, double precision FPU multicellular processor core c the core is 24 MFlops/MHz. Calculated value of power consumption

MULTICLET C1

Multicellular processor core MULTICLET C1 is oriented at ultra-low power **C**onsumption and simultaneou
multicellular architecture and possesses the ability of natural implementation of parallelism. Architecture
during program processing without the use of specialized standard cell libraries. MULTICLET P2 is fully s

Nomenclature	Implementation	Description
MCc040C1	FPGA	4-cells, 32bit, fixed point processor core contains ALU in each cell. F is 3.2 MIPS/MHz. Calculated value of power consumption on 180nm

MULTICLET R1

Processor core MULTICLET R1 is based on the unique multicellular architecture and provides natural im
architecture possesses the ability of dynamic **R**econfiguration by means of which core's cells can simulta
processors based on multicellular architecture possess such ability. MULTICLET R1 is fully synthesizabl

Nomenclature	Implementation	Description
MCc042R1	SoC	4-cells, 32/64bit, double precision FPU multicellular processor core c the core is 24 MFlops/MHz. Calculated value of power consumption

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MCc042R1-1	SoC	4-cell, 32/64bit, double precision FPU multicellular processor core co the core is 24 MFlops/MHz. Calculated value of power consumption

MULTICLET L1

Processor core MULTICLET L1 possesses **L**iveness ability and is oriented at maximum performance wit
consumption. The core is based on the unique multicellular architecture and possesses the attribute of n
tolerance is an inborn attribute of the core and is resulted from core architecture. “Fault tolerance” is an a
1, 2 or 3 cells fail to perform while the performance is reduced. Consequently, the core posses a system
level called "Rad-Hard by Design". MULTICLET L1 is fully synthesizable.

Nomenclature	Implementation	Description
MCc042L1	RTL	4-cells, 32/64bit, double precision FPU processor core contains ALU 24 MFlops/MHz. Calculated value of power consumption on 180 nm

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